

CLAIMS

What is claimed is:

1. A semiconductor capacitor having a lower electrode, a dielectric layer and an upper electrode, wherein the upper electrode comprises a deposition structure including a doped polysilicon layer formed between a first undoped polysilicon layer and a second undoped polysilicon layer.
2. The capacitor, as defined in claim 1, wherein the first and second undoped polysilicon layers are formed at a thickness of less than 1000A.
3. The capacitor, as defined in claim 1, wherein the doped polysilicon layer is formed at a thickness between 1800A and 2500A.
4. The capacitor, as defined in claim 1, wherein an additional metal pattern is deposited over the upper electrode.
5. The capacitor, as defined in claim 4, wherein the metal pattern is constructed in a deposition structure including a blocking metal layer and an aluminum layer.
6. The capacitor, as defined in claim 5, wherein the blocking metal layer is constructed in a structure including a Ti layer and a TiN layer.

7. A method for fabricating a capacitor having a lower electrode, a dielectric layer and upper electrode, wherein the upper electrode is formed according to the following steps:

forming a first undoped polysilicon layer;

forming a doped polysilicon layer on the first undoped polysilicon layer; and

forming a second undoped polysilicon layer on the doped polysilicon layer.

8. The method, as defined in claim 7, wherein the first and second undoped polysilicon layers are formed at a thickness of less than 1000A.

9. The method, as defined in claim 7, wherein the doped polysilicon layer is formed at a thickness between 1800A and 2500A.

10. The method, as defined in claim 7, wherein the second undoped polysilicon layer is formed at the same temperature as that of the doped layer without any breakup of vacuum following formation of the doped polysilicon layer.

11. The method, as defined in claim 7, wherein an additional metal pattern is deposited over the upper electrode.

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